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parallel load input = 1,
the clock pulses go
through the AND gate
and the data inputs are
loaded into the register
when the parallel load
input = 0, the output of
the AND gate remains

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at 0. 2.10. The buffer gate does not perform logic. It is used for signal amplification of the clock input.

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basically a machine
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than -1, so the system never has any gain to compensate for noise.

Exercise 1.81 The circuit functions as a buffer with logic levels $V_{IL} = 1.5$; $V_{IH} = 1.8$; $V_{OL} = 1.2$; $V_{OH} = 3.0$.

It can receive inputs from LVCMOS and LVTTL gates be- ...

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